DIGITAL VECTOR CONTROL CHIP SET AT Q BAND FOR COMMUNICATION PHASED ARRAY

M. LAJUGIE, H. BROUZES (*), F. VILLAIN(**)

THOMSON-CSF MICROELECTRONIQUE - 29 Avenue Carnot - 91 349 MASSY - FRANCE
(*) Now with SIGNAAL, HENGELO - THE NETHERLANDS
(**) Now with HITTITE MICROWAVES CORP., WOBURN - MA - USA

ABSTRACT :

Two chips have been developed for vector control at Q band. The five bit -360° MMIC true phase shifter and the six bit -32 dB attenuator have been manufactured and tested in 0.25 µm P-HEMT (UMS, PH25 Process). Maximum measured errors on single bits are 4° / 2dB. Combined insertion loss stays below 15 dB. Communication phased array system are made possible using such MMICs.

I - INTRODUCTION :

The growing demand for smarter communication systems and the race towards free millimeter waves spectrum pushes the need for new MMIC development. We report on the design and measurement of a complete vector control chip set which can be used in various equipments such as phased array antennas.

Very few millimeterwave monolithic phase shifters have been reported earlier, and no digital attenuator has been published to our knowledge, although microwaves frequency phase shifters and attenuators are widely available ([1],... [9]). This manufactured chip set is the first to yield a full 5 bit pure phase/32dB 6 bit module control in millimeter waves.

The MMICs are digitally controlled to decrease the overall system cost (DA converters, calibration circuits, temperature compensation devices...). The whole structure is built around cold FETs thus yielding negligible power consumption.

The PH25 technology from UMS (0.25 µm P-HEMT) has been chosen for this control application for three main reasons:

- The quality factor of the cold FETs is comparable to low-frequency switch processes,
- This process is fully characterized up to 60 GHz with scalable cold FETs models,
- The ultimate goal is a fully integrated multifunction chip with intermediate amplifier stages, and until then chip sets comprising low-noise and medium power amplifiers will be manufactured on same wafers.

Control chips were implemented on a First Run Multichip / Multiversion Mask Set, the two reported ones are the most significant.

II - PHASE SHIFTER DESIGN :

The phase shifter chip consists of five true phase bits, yielding phase control with 360° dynamic and 11.25° resolution across the 43.5-45.5 GHz frequency band.

Electrical structure of all phase bits have been carefully chosen for optimum performance at Q-band, taking also into account modeling uncertainties and process sensitivity (some topologies were disregarded due to high process sensitivities).

Communication applications for phased array antennas lead to stringent requirements on time delay variations across bandwidth and states if instantaneous wide band operation is needed (frequency agility for example). This led to eliminate any option based upon switched line phase shifter.

The smallest phase bits are twin loaded line bits, the 45° bit consisting in optimized two 22.5° bits in series. On those bits, both transmission line parameters and FET size (4 x 100 & 4 x 77 µm) were optimized.

The 90° and 180° bit are switched filter types, makingu se of a simple $\lambda/4$ resonated shunt 2 x 58 µm FET for the switch.

EM simulator has been extensively used for all coupled discontinuities and via hole effects.

Each bit has first been optimized against process variations. Then the bit order was carefully chosen for minimal bit to bit interaction. The complete chip has finally been optimized with its bonding wires for minimal rms error, insertion loss and VSWR.

Chip layout is presented in fig 1. Overall size is 7.63 x 2.74 mm². This first pass size is expected to be decreased after redesign.

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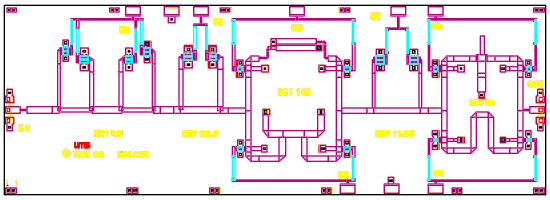

Fig. 1 : Phase Shifter Layout

III - MEASURED PERFORMANCE :

6 fully functional phase shifter chips have been characterized on-wafer.

The circuit exhibits wide band capability, with more than 5 GHz usable bandwidth.

Within the nominal 43.5 - 45.5 GHz bandwidth, the overall insertion loss, presented in fig 2, is somewhat better than the simulated one, with a maximum value of 9 dB. The insertion loss variation across states, frequency and chips stays below ± 1 dB. Return loss stays below -10 dB, and should improve after bonding.

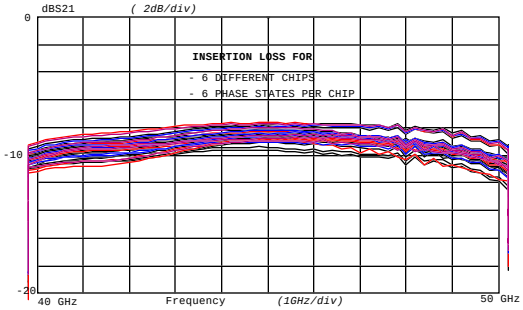

Fig. 2 : OW Measured Phase Shifter

Fig 3 to 7 show the measured performance of the six chips for the elementary phase bits.

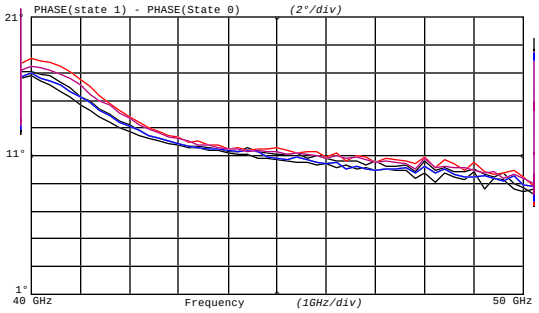

Fig.3:OW measured 11.25° Bit

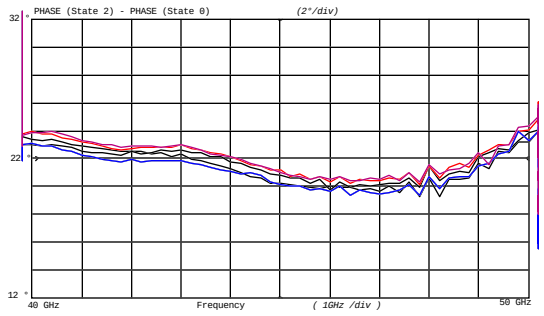

Fig.4: OW measured 22.5° Bit

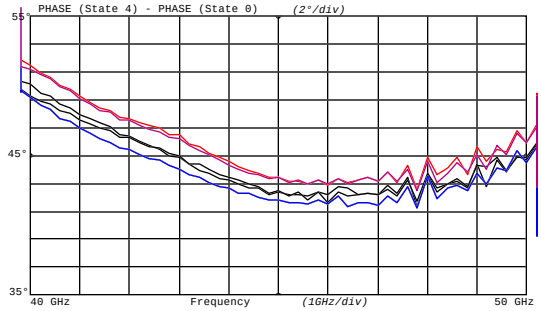

Fig.5: OW measured 45° Bit

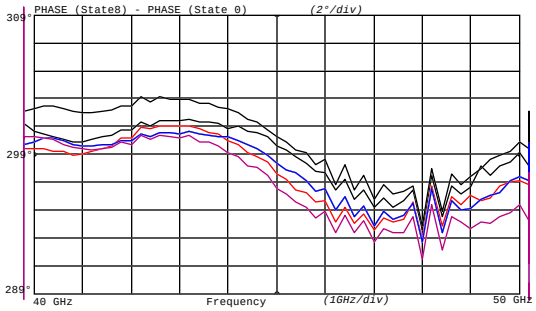

Fig.6: OW measured 90° Bit

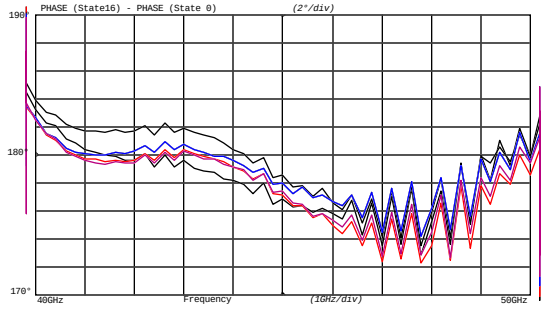

Fig.7: OW measured 180° Bit

The achieved phase precision and reproducibility is the following:

-11.25°	bit :	+ 0.75/ -0.7°
-22.5°	bit :	+ 0 / -2.7°
- 45°	bit :	+ 0 / -3.5°
- 180°	bit :	+ 4 / -4.5°

The 90° bit is off phase, yielding a nominal phase shift centred around 300°, which is a measurement problem.
Phase reproducibility is + 3 / -5°.

IV - ATTENUATOR DESIGN :

The 6 bits digital attenuator has been designed to yield 32 dB of dynamic range in 0.5 dB steps over the 43.5 - 45.5 GHz frequency band.
Attenuator topology has been chosen to reduce the sensitivity to process variations, and to stay as simple as possible (simulation accuracy, real-estate optimization...).
Although it basically employs a T-configuration, the new attenuator distributes a segmented gate shunt FET into nine cells interconnected by high impedance transmission lines. The different attenuation values are obtained through the RF signal leakage in the RON resistor of FET in ON state. This leakage level is adjusted for the smallest attenuation bits by adding an additional series resistor. At minimum attenuation setting, when shunt FETs may be represented as capacitors, the distributed structure absorbs the FET capacitance into an artificial transmission line which guarantees a good match.
Individual FET sizes range from 1 x 20 µm to 1 x 55 µm, with a total gate periphery of 255 µm. Time delay has been checked not to degrade phase shifter performance.
Having selected the individual attenuation bits, the cascaded arrangement was computer optimized to achieve the lowest possible rms error. Chip layout is presented in fig. 8. Circuit size is 2.74 x 2.42 mm².

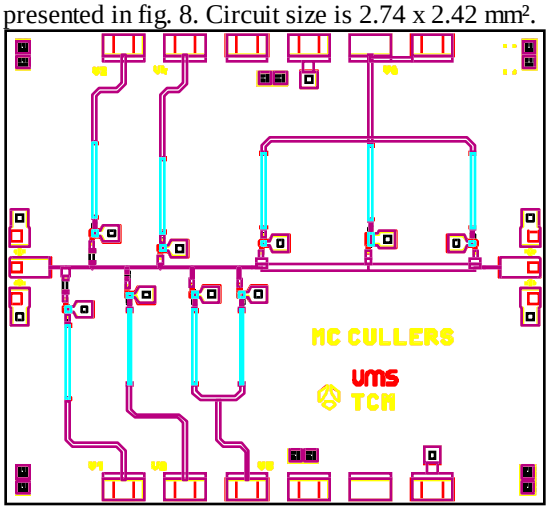

Fig. 8 : Attenuator Layout

V - MEASURED PERFORMANCE :

5 fully functional attenuator chips have been characterized on-wafer.
Chip performance is wide band, with a usable bandwidth of more than 10 GHz.
The overall insertion loss presented in fig 9 is here also better than simulated, with a maximum value of 3.5 dB. Return loss stays below the simulated - 10 dB.

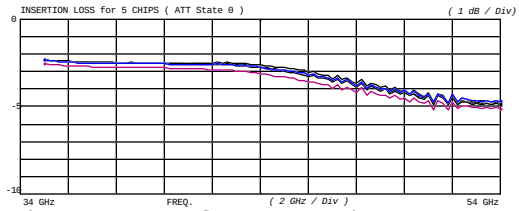

Fig. 9 : On Wafer Measured Attenuator Insertion Loss ATT State 0 - Ref.

In the nominal 43.5 - 45.5 GHz bandwidth, attenuation performance, presented in fig 10 to 15, can be summarized as follows, including chip to chip and frequency dispersion :

- 16 dB	bit :	15.2dB ± 0.4 dB
- 8 dB	bit :	7.4dB ± 0.2 dB
- 4 dB	bit :	4.3dB ± 0.3 dB
- 2 dB	bit :	1.7dB ± 0.3 dB
- 1 dB	bit :	1.1dB ± 0.08dB
- 0.5dB	bit :	0.59dB ± 0.07dB

So rms error is expected to stay within 0.4 to 0.9 dB.

VI - CONCLUSION :

A first run of two chips for vector control at Q band has been manufactured and tested.
These two chips provide 5 bit phase control / 6 bit attenuation control with 360° / 32 dB dynamic range in more than 5 GHz bandwidth, and are the first reported ones of their type. Overall insertion loss for the two chips stays below 15 dB (for the 11 bits). The phase and amplitude accuracy demonstrated are fully compatible with a direct implementation within actual systems.

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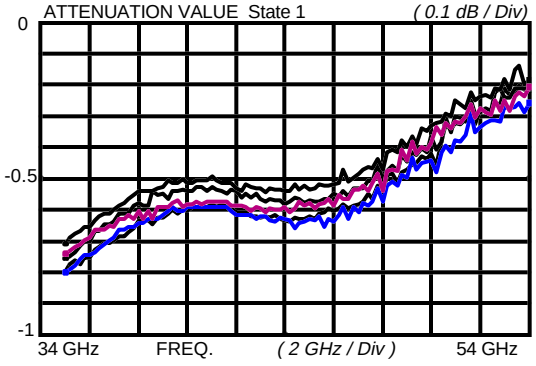

Fig. 10 : OW ATTENUATION Bit 0.5 dB

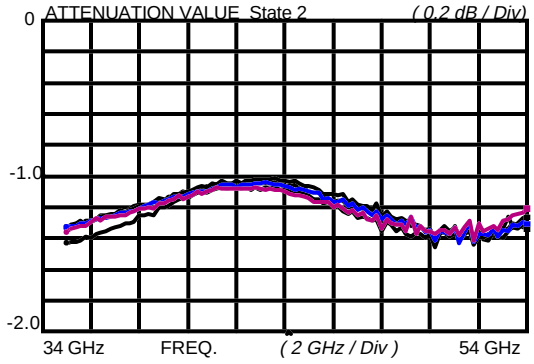

Fig. 11 :OW ATTENUATION Bit 1 dB

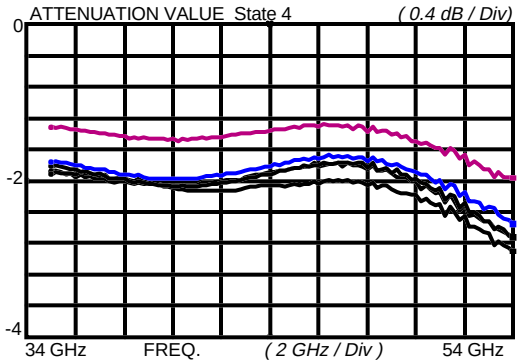

Fig. 12 : OW ATTENUATION Bit 2 dB

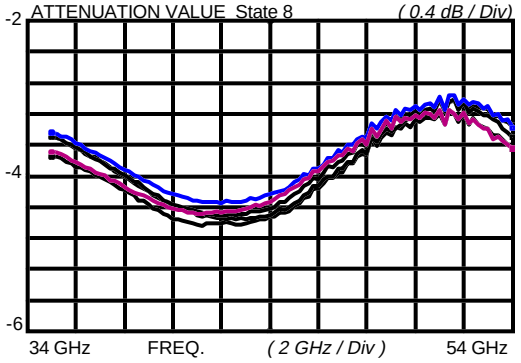

Fig. 13 : OW ATTENUATION Bit 4 dB

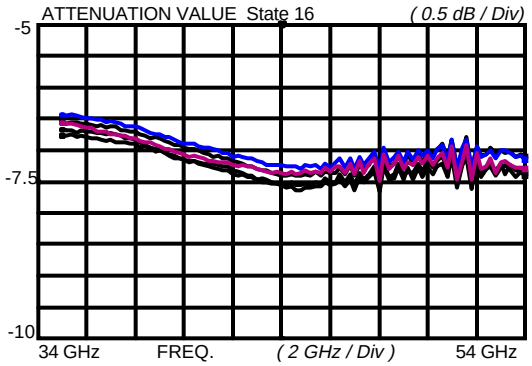

Fig. 14 : OW ATTENUATION Bit 8 dB

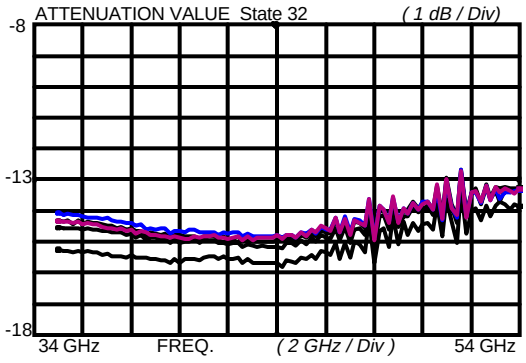

Fig. 15 : OW ATTENUATION Bit 16 dB